



Data sheet acquired from Harris Semiconductor
SCHS085E – Revised September 2003

CMOS Programmable Timer High Voltage Types (20V Rating)

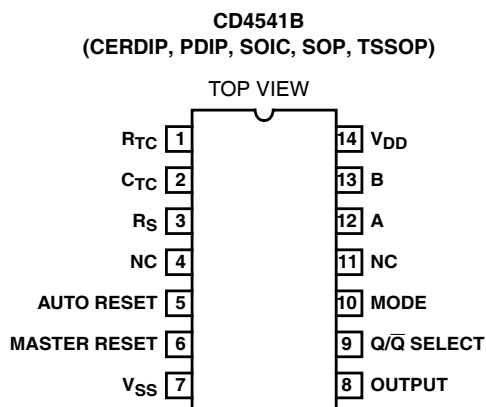
Features

- Low Symmetrical Output Resistance, Typically 100Ω at V_{DD} = 15V
- Built-In Low-Power RC Oscillator
- Oscillator Frequency Range DC to 100kHz
- External Clock (Applied to Pin 3) can be Used Instead of Oscillator
- Operates as 2^N Frequency Divider or as a Single-Transition Timer
- Q/ \bar{Q} Select Provides Output Logic Level Flexibility
- AUTO or MASTER RESET Disables Oscillator During Reset to Reduce Power Dissipation
- Operates With Very Slow Clock Rise and Fall Times
- Capable of Driving Six Low Power TTL Loads, Three Low-Power Schottky Loads, or Six HTL Loads Over the Rated Temperature Range
- Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- 5V, 10V, and 15V Parametric Ratings
- Meets All Requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Description

CD4541B programmable timer consists of a 16-stage binary counter, an oscillator that is controlled by external R-C components (2 resistors and a capacitor), an automatic power-on reset circuit, and output control logic. The counter increments on positive-edge clock transitions and can also be reset via the MASTER RESET input.

Pinout



The output from this timer is the Q or \bar{Q} output from the 8th, 10th, 13th, or 16th counter stage. The desired stage is chosen using time-select inputs A and B (see Frequency Select Table).

The output is available in either of two modes selectable via the MODE input, pin 10 (see Truth Table). When this MODE input is a logic "1", the output will be a continuous square wave having a frequency equal to the oscillator frequency divided by 2^N. With the MODE input set to logic "0" and after a MASTER RESET is initiated, the output (assuming Q output has been selected) changes from a low to a high state after 2^{N-1} counts and remains in that state until another MASTER RESET pulse is applied or the MODE input is set to a logic "1".

Timing is initialized by setting the AUTO RESET input (pin 5) to logic "0" and turning power on. If pin 5 is set to logic "1", the AUTO RESET circuit is disabled and counting will not start until after a positive MASTER RESET pulse is applied and returns to a low level. The AUTO RESET consumes an appreciable amount of power and should not be used if low-power operation is desired. For reliable automatic power-on reset, V_{DD} should be greater than 5V.

The RC oscillator, shown in Figure 2, oscillates with a frequency determined by the RC network and is calculated using:

$$f = \frac{1}{2.3 R_{TC} C_{TC}}$$

Where f is between 1kHz and 100kHz and R_S ≥ 10kΩ and ≈ 2R_{TC}

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4541BF3A	-55 to 125	14 Ld CERDIP
CD4541BE	-55 to 125	14 Ld PDIP
CD4541BM	-55 to 125	14 Ld SOIC
CD4541BMT	-55 to 125	14 Ld SOIC
CD4541BM96	-55 to 125	14 Ld SOIC
CD4541BNSR	-55 to 125	14 Ld SOP
CD4541BPW	-55 to 125	14 Ld TSSOP
CD4541BPWR	-55 to 125	14 Ld TSSOP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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Functional Diagram

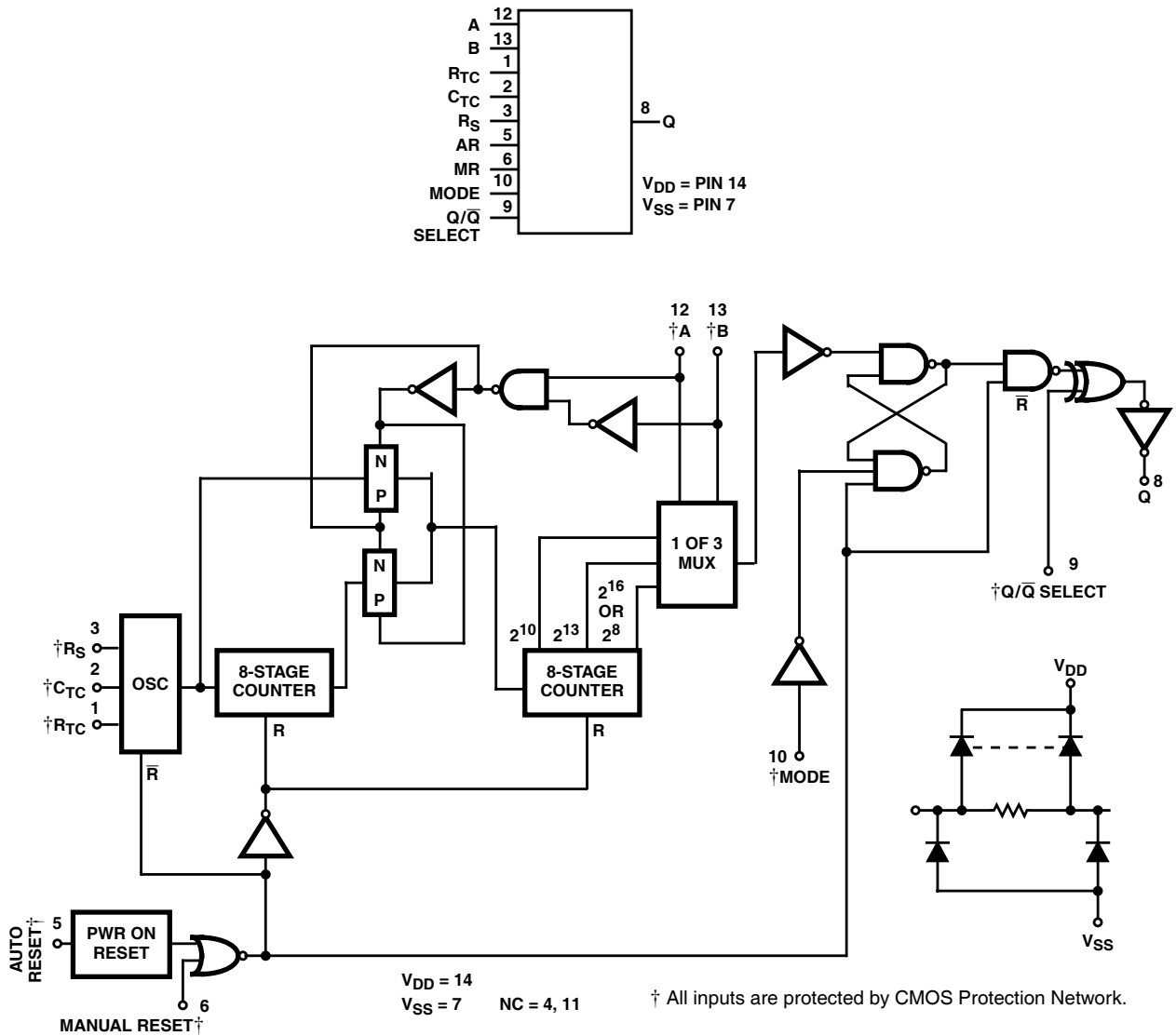


FIGURE 1.

FREQUENCY SELECTION TABLE

A	B	NO. OF STAGES N	COUNT 2^N
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

PIN	STATE	
	0	1
5	Auto Reset On	Auto Reset Disable
6	Master Reset Off	Master Reset On
9	Output Initially Low After Reset (Q)	Output Initially High After Reset (Q)
10	Single Transition Mode	Recycle Mode

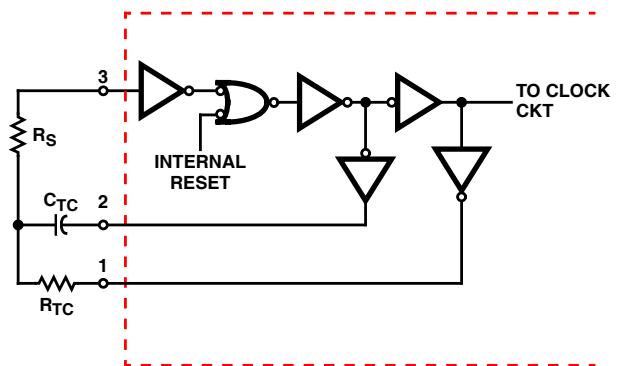


FIGURE 2. RC OSCILLATOR CIRCUIT

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Absolute Maximum Ratings

DC Supply - Voltage Range, V_{DD}
 Voltages Referenced to V_{SS} Terminal -0.5V to +20V
 Input Voltage Range, All Inputs -0.5V to $V_{DD} + 0.5V$
 DC Input Current, Any One Input $\pm 10mA$
 Device Dissipation Per Output Transistor
 For T_A = Full Package Temperature Range
 (All Package Types) 100mW

Operating Conditions

Temperature Range T_A -55°C to 125°C
 Supply Voltage Range
 For T_A = Full Package Temperature Range 3V (Min), 18V (Typ)

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1)
 PDIP package 80°C/W
 SOIC package 86°C/W
 SOP package 76°C/W
 TSSOP package 113°C/W
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range (T_{STG}) -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s)
 At Distance 1/16in \pm 1/32in (1.59mm \pm 0.79mm)
 from case for 10s Maximum 265°C
 (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Specifications

PARAMETER	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	85	125	25			
								MIN	TYP	MAX	
Quiescent Device Current, (Note 2) I_{DD} (Max)	-	0, 5	5	5	5	150	150	-	0.04	5	μA
	-	0, 10	10	10	10	300	300	-	0.04	10	μA
	-	0, 15	15	20	20	600	600	-	0.04	20	μA
	-	0, 20	20	100	100	3000	3000	-	0.08	100	μA
Output Low (Sink) Current I_{OL} (Min)	0.4	0, 5	5	1.9	1.85	1.26	1.08	1.55	3.1	-	mA
	0.5	0, 10	10	5	4.8	3.3	2.8	4	8	-	mA
	1.5	0, 15	15	12.6	12	8.4	7.2	10	20	-	mA
Output High (Source) Current, I_{OH} (Min)	4.6	0, 5	5	-1.9	-1.85	-1.26	-1.08	-1.55	-3.1	-	mA
	2.5	0, 5	5	-6.2	-6	-4.1	-3	-5	-10	-	mA
	9.5	0, 10	10	-5	-4.8	-3.3	-2.8	-4	-8	-	mA
	13.5	0, 15	15	-12.6	-12	-8.4	-7.2	-10	-20	-	mA
Output Voltage: Low-Level, V_{OL} (Max)	-	0, 5	5	-	-	0.05	-	-	0	0.05	V
	-	0, 10	10	-	-	0.05	-	-	0	0.05	V
	-	0, 15	15	-	-	0.05	-	-	0	0.05	V
Output Voltage: High-Level, V_{OH} (Min)	-	0, 5	5	-	-	4.95	-	4.95	5	-	V
	-	0, 10	10	-	-	9.95	-	9.95	10	-	V
	-	0, 15	15	-	-	14.95	-	14.95	15	-	V
Input Low Voltage, V_{IL} (Max)	0.5, 4.5	-	5	-	-	1.5	-	-	-	1.5	V
	1, 9	-	10	-	-	3	-	-	-	3	V
	1.5, 13.5	-	15	-	-	4	-	-	-	4	V

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Electrical Specifications (Continued)

PARAMETER	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	85	125	25			
								MIN	TYP	MAX	
Input High Voltage, V _{IH} (Min)	0.5, 4.5	-	5	-		3.5		3.5	-	-	V
	1, 9	-	10	-		7		7	-	-	V
	1.5, 13.5	-	15	-		11		11	-	-	V
Input Current, I _{IN} (Max)	-	0, 18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

NOTE:

2. With AUTO RESET enabled, additional current drain at 25°C is:
 7μA (Typ), 200μA (Max) at 5V;
 30μA (Typ), 350μA (Max) at 10V;
 80μA (Typ), 500μA (Max) at 15V

Dynamic Electrical Specifications $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ns}$, $C_L = 50\text{pF}$, $R_L = 200\text{k}\Omega$

PARAMETER	SYMBOL	V _{DD} (V)	MIN	TYP	MAX	UNITS
Propagation Delay Times Clock to Q	(2 ⁸) t _{PHL} , t _{PLH}	5	-	3.5	10.5	μs
		10	-	1.25	3.8	μs
		15	-	0.9	2.9	μs
	(2 ¹⁶) t _{PHL} , t _{PLH}	5	-	6.0	18	μs
		10	-	3.5	10	μs
		15	-	2.5	7.5	μs
Transition Time	t _{THL}	5	-	100	200	ns
		10	-	50	100	ns
		15	-	40	80	ns
	t _{TLH}	5	-	180	360	ns
		10	-	90	180	ns
		15	-	65	130	ns
MASTER RESET, CLOCK Pulse Width		5	900	300	-	ns
		10	300	100	-	ns
		15	225	85	-	ns
Maximum Clock Pulse Input Frequency	f _{CL}	5	-	1.5	-	MHz
		10	-	4	-	MHz
		15	-	6	-	MHz
Maximum Clock Pulse Input Rise or Fall time	t _r , t _f	5, 10, 15	Unlimited			μs

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Digital Timer Application

A positive pulse on MASTER RESET resets the counters and latch. The output goes high and remains high until the number of pulses, selected by A and B, are counted. This circuit is retriggerable and is as accurate as the input frequency. If additional accuracy is desired, an external clock can be used on pin 3. A setup time equal to the width of the one-shot output is required immediately following initial power up, during which time the output will be high.

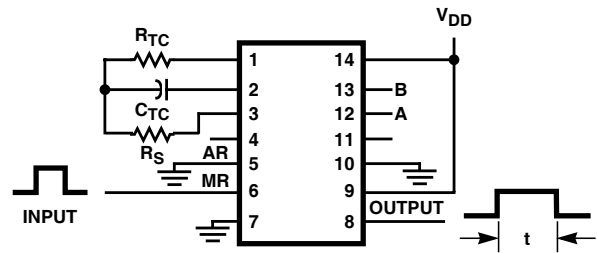


FIGURE 3. DIGITAL TIMER APPLICATION CIRCUIT